WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit device, comprising:

a latch provided on the output of a memory circuit or on the input of a logic circuit,

wherein said latch includes a signal selector for switching between feedback signal of normal operation and test signal of test operation in compliance with the operation mode signal to send out to a feedback loop.

2. A semiconductor integrated circuit device according to claim 1, wherein:

said latch is provided at the output of said memory,

said signal selector is controlled by said operation mode signal for sending out to said feedback loop either one of the latch output signal as the feedback signal or the input signal to said memory as the test signal.

3. A semiconductor integrated circuit device according to claim 1, wherein:

said latch is provided at the output of said memory,

said signal selector includes a logic gate for receiving said operation mode signal and latch output signal, and

said logic gate outputs fixedly an output signal of

a predetermined level by the operation mode signal in the test mode operation for sending out to a feedback loop as said test signal.

4. A semiconductor integrated circuit device according to claim 1, wherein:

said latch is provided at the output of said memory;

said latch has a first switch for sending the read-out signal from a memory cell in said memory to an input terminal of a first inverter under the control of switch control signal, a second inverter for receiving the output signal of said first inverter on the input terminal, and a second switch for sending the output signal of said second inverter to the input terminal of said first inverter under the control of said switch control signal, and said latch outputs a latch output signal from the output terminal of said second inverter;

said signal selector has a third switch for sending the input signal fed to said memory to the input terminal of said first inverter as the test signal under the switching control of said switch control signal, and a signal generator for generating said switch control signal;

said signal generator turns off said third switch in the normal operation by said operation mode signal to perform a complementary switching control of said first and

second switches by using clock pulses as said switch control signal, and turns off said first and second switches and turns on said third switch in the test operation by said operation mode signal.

5. A semiconductor integrated circuit device according to claim 1, wherein:

said latch is provided at the input of said logic;

said latch includes a first latch for receiving the input signal in the normal operation and a second latch for generating the signal input to said logic upon reception of the output from said first latch; and

said signal selector is provided in the feedback loop of said first latch.

6. A semiconductor integrated circuit device according to claim 5, wherein:

said first latch has a first switch for sending said input signal to the input terminal of a first inverter under the switching control signal, a first clocked inverter for receiving the output signal from said first inverter on the input terminal under the control of clock pulses, and a second switch for sending the output signal from said first clocked inverter to the input terminal of said first inverter under the control of said switching control signal;

said second latch has a circuit under the control of said clock pulses for performing signal collection and signal retention in complementary to said first latch, a second inverter for generating output signal to the input of said logic, and a third inverter for generating output signal for test scan;

said signal selector has a second clocked inverter under the control of said switch control signal for receiving the test input signal on the input terminal, a third switch for sending the output signal from said second clocked inverter to the input of said second switch under the switching control of said clock pulses, and a signal generator for generating said switching control signal;

wherein said signal generator turns off said second clocked inverter by said operation mode signal during the normal operation, passing said clock pulses to said first and second switches as said switch control signal, in order to perform the complementary operation of signal collection and signal retention in response to the input signal by the first and second latches; and

wherein said signal generator turns off said first switch and turns on said second switch during the test mode in accordance with said operation mode signal, in order to perform the complementary operation of signal collection and signal retention by the first and second latches in

response to the test input passing through said second clocked inverter in the normal operation mode.

7. A semiconductor integrated circuit device, comprising a circuit, said circuit operating in either

a first mode for operating as said latch; or

a second mode for passing through the signal input from a signal switching circuit provided in the feedback loop of said latch.

8. A semiconductor integrated circuit device according to claim 7, wherein:

said first mode is the normal operation mode, and

said second mode is the test mode.

9. A semiconductor integrated circuit device, comprising:

a first input node;

a transfer gate coupled to said first input node;

an output node coupled to said transfer gate;

a feedback loop provided between said first transfer gate and said output node; and

a second input node coupled to said feedback loop;

said first transfer gate in a first mode transferring data input from said input node to said output node based on clock signals, said first transfer gate in a second mode

disconnecting said input node from said output node; and

data being input to said second input node in said second mode.

10. A semiconductor integrated circuit device according to claim 9, wherein:

said semiconductor integrated circuit device further comprises a multiplexor provided in said feedback loop,

said multiplexor coupled to said output node and said second input node to select said output node in said first mode and to select said second input node in said second mode.

11. A semiconductor integrated circuit device according to claim 9, wherein:

said semiconductor integrated circuit device further comprises a second transfer gate provided in said feedback loop,

said second transfer gate determining whether or not to feed back the data transferred to said output node based on said clock signal in said first mode, and transferring to said output node the data input to said second input node in said second mode.